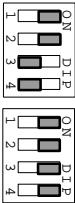
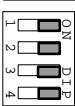


89C2051 Programming unit Quick Reference

Standard Settings



Normal operation
Erase, Program on
(May be verified)



Security operation
Erase,Prog.Lock on
(Reads as 'Blank')

LED Status Indication

- Red/Grn on - Idle
- Red/Grn flash - Blank
- Grn solid - Good data
- Red flash - Bad chip
- Red solid - data, not CKS'd, or failed prog

Test & Programming

To Test an AT89C2051, insert it in the socket and push "TEST". LEDs indicate the device status.

To Program, set dipswitches and download the file. Test and verification is automatic. LEDs indicate the programming result.

Serial Protocol

Downloaded files should be Intel™ Hexformat, Serial at 9600 Baud, 8 data bits, 2 stop bits, no parity.

Typical commands:

Mode COM1:9600,N,8,2

Copy Myfile.hex COM1

Operation notes

Position the AT89C2051 with pin 1 to the top left of the socket.
Use only the DC power source supplied with your unit.
Do not operate the device where there is a danger of short circuit.
Do not write to the same byte twice in a Hex file.
Operate at the Serial settings specified - 2 stop bits is important.
Other dipswitch combinations are valid - ALL OFF is verify chip.

AirBorn
ELECTRONICS

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P O Box 1491, North Sydney,
NSW 2059, Australia

89C2051 Microprocessor Quick Reference

89C2051

Pinout

RST	□	VCC
(RxD) P3.0	□	P1.7
(TxD) P3.1	□	P1.6
XTAL2	□	P1.5
XTAL1	□	P1.4
(INT0) P3.2	□	P1.3
(INT1) P3.3	□	P1.2
(TO) P3.4	□	P1.1 (AIN1)
(T1) P3.5	□	P1.0 (AIN0)
GND	□	P3.7

TOP VIEW

89C2051 Features

8051 instruction set & I/O: 8051 serial, timers, interrupts. 128 bytes RAM, 2k FLASH Program memory, 2.7-6v Vcc. Ports P1.0,P1.1 have no pullups and feed an analog comparator "AIN" internally read on P3.6.

8051 Mnemonics

add a,Rn	anl a,Rn	mov a,Rn	push Di	jc Rel
add a,Di	anl a,Di	mov a,@Ri	pop Di	jnc Rel
add a,@Ri	anl a,@Ri	mov a,#dat	xch a,Rn	jb Bi,Rel
add a,#dat	anl a,#dat	mov Rn,a	xch a,Di	jnb Bi,Rel
addc	anl Di,a	mov Rn,Di	xch a,@Ri	jbc Bi,Rel
subb	anl Di,#dat	mov Rn,#d	xchda,@Ri	acall Addr
	orl	mov Di,a	ret	
inc a	xrl	mov Di,Rn	clr c	reti
inc Rn		mov Di,Di	clr bit	ajmp Addr
inc Di	clr a	movDi,@Ri	setb	jmp @a+DP
inc @Ri	cpl a	mov Di,#da	cpl	jz Rel
dec	rl a	mov @Ri,a	anl c,Bi	jnz Rel
	rlc a	mov @Ri,Di	anl c,/Bi	cjne a,Di,Rel
inc dptr	rr a	mov @Ri,#d	orl	cjne a,#Da,Rel
mul ab	rrc a	movDPTR,#d		cjneRn,#D,Rel
div ab	swap a	movca@a+DP	mov C,Bi	cjne @Ri,#Da,Rel
da a		nop	movca@a+PC	djnz Rn,Rel
			mov Bi,C	djnz Di,Rel

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(INT1) P3.3	□	P1.2
(TO) P3.4	□	P1.1 (AIN1)
(T1) P3.5	□	P1.0 (AIN0)
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